

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	10/777,012
Filing Date	02/11/2004
First Named Inventor	Richard W. Foote
Art Unit	2632
Examiner Name	Not Yet Assigned
Attorney Docket Number	P05792

Sheet	1	of	4
-------	---	----	---

[illegible][illegible]

**Examiner
Signature**

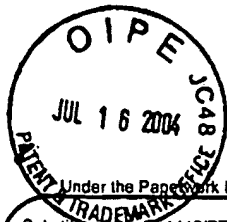
Date
Considered

9/21/05

*EXAMINER: Initial if reference considered whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.



PTO/SB/08B (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	10/777,012
Filing Date	02/11/2004
First Named Inventor	Richard W. Foote
Art Unit	2632
Examiner Name	Not Yet Assigned
Attorney Docket Number	P05792

Sheet

2

of

4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
SSF	BA	M. Shimizu et al., "A Novel Polysilicon Source/Drain Transistor with Self-Aligned Silicidation", LSI R&D Laboratory, Mitsubishi Electric Corporation, Pp. 11-12.	
SSF	BB	S. Hsia et al., "Polysilicon Oxidation Self-Aligned MOS (POSA MOS) - A New Self-Aligned Double Source/Drain Ion Implantation Technique for VLSI", IEEE Electron Device Letters, Vol. EDL-3, No. 2, February 1982, Pp. 40-42.	
SSF	BC	Kamal Rajkanan et al., "A High-Performance BICMOS Technology with Double-Polysilicon Self-Aligned Bipolar Devices", IEEE Electron Device Letters, Vol. EDL-8, No. 11, November 1987, Pp. 509-511.	
SSF	BD	Tiao-Yuan Huang et al., "A MOS Transistor with Self-Aligned Polysilicon Source-Drain", IEEE Electron Device Letters, Vol. EDL-7, No. 5, May 1986, Pp. 314-316.	
SSF	BE	C. S. Oh et al., "A New MOSFET Structure with Self-Aligned Polysilicon Source and Drain Electrodes", IEEE Electron Device Letters, Vol. EDL-5, No. 10, October 1984, Pp. 400-402.	
SSF	BF	W. Josquin et al., "The Integration of Double-Polysilicon NPN Transistors in an Analog BiCMOS Process", Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988 Pp. 149-152.	
SSF	BG	Tunenori Yamauchi et al., "High Speed BICMOS Technology with Emitter-base Self-aligned Structure", Bipolar IC Division Fujitsu Limited, Pp. 155-158.	
SSF	BH	Kwang Soo Kim et al., Bipolar-Complementary-Metal-Oxide-Semiconductor (BiCMOS) Technology with Polysilicon Self-Aligned Bipolar Devices", Japanese Journal of Applied Physics, Vol. 30, No. 10, October 1991, Pp. 2459-2465.	
SSF	BI	Masahiro Shimizu et al., "A Novel CMOS Structure with Polysilicon Source/Drain (PSD) Transistors by Self-Aligned Silicidation", IEICE Trans. Electron, Vol. E76-C, No. 4, April 1993, Pp. 532-540.	
SSF	BJ	M. K. Moravvej-Farshi et al., "Novel Self-Aligned Polysilicon-Gate MOSFETS with Polysilicon Source and Drain, Solid-State Electronics, Vol. 30, No. 10, 1987, Pp. 1053-1062.	

Examiner
Signature

Date

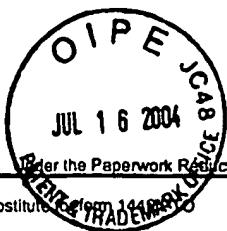
Considered

9/21/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.



PTO/SB/088 (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known	
		Application Number	10/777,012
		Filing Date	02/11/2004
		First Named Inventor	Richard W. Foote
		Art Unit	2632
		Examiner Name	Not Yet Assigned
Sheet 3	of 4	Attorney Docket Number	P05792

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
STF	CA	W. R. Burger et al., "An Advanced Self-Aligned BiCMOS Technology for High Performance 1-MegaBit ECL I/O SRAM's", National Semiconductor Corp., Puyallup Technology Development, 1989.	
STF	CB	James Warnock et al., "BiCMOS Technology with 60-Ghz n-p-n Bipolar and 0.25-µm CMOS", IEEE Electron Device Letters, Vol. 13, No. 11, November 1992, Pp. 578-580.	
STF	CC	J. D. Hayden et al., "Integration of a Double Polysilicon, Fully Self-Aligned Bipolar Transistor into a 0.5µm BiCMOS Technology for Fast 4MBit SRAMs", Advanced Products Research and Development Laboratory, Motorola Inc., IEEE 1991 Bipolar Circuits and Technology Meeting, Pp. 17-20.	
STF	CD	T. C. Mele et al., "A High Performance 0.5µm BiCMOS Triple Polysilicon Technology for 4mb Fast SRAMs", Advanced Products Research and Development Laboratory, Motorola Inc., IEEE 1990.	
STF	CE	Kenneth O'Peter Garone et al., "A Double-Polysilicon Self-Aligned npn Bipolar Process (ADRF) with Optional NMOS Transistors for RF and Microwave Applications", 1994 Bipolar/BiCMOS Circuits & Technology Meeting, Pp. 221-224.	
STF	CF	Alain Chantre et al., "Identification of a Corner Tunneling Current Component in Advanced CMOS-Compatible Bipolar Transistors", IEEE Transactions on Electron Devices, Vol. 38, No. 1, January 1991, Pp. 107-110.	
STF	CG	K. Ishimaru et al., "Bipolar Installed CMOS Technology without Any Process Step Increase for High Speed Cache SRAM", IEEE 1995.	
STF	CH	Shih Wei Sun et al., "Selective-Polysilicon Emitter, Self-Aligned Bipolar Structure for BiCMOS VLSI Applications", Motorola Inc., Advanced Products Research and Development Laboratory, Pp. 55-56.	
STF	CI	Tzu-Yin Chin et al., "The Design and Characterization of Nonoverlapping Super Self-Aligned BiCMOS Technology", IEEE Transactions on Electron Devices, Vol. 38, No. 1, January 1991, Pp. 141-150.	
STF	CJ	Tadanori Yamaguchi et al., "Process Integration and Device Performance of a Submicrometer BiCMOS with 16-Ghz ft. Double Poly-Bipolar Devices", IEEE Transactions on Electron Devices, Vol. 36, No. 5, May 1989, Pp. 890-896.	

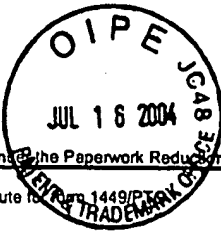
Examiner Signature		Date Considered	9/21/05
--------------------	--	-----------------	---------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.



PTO/SB/08B (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for Form 1449/PTO
TRADEMARK OFFICE**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	10/777,012
Filing Date	02/11/2004
First Named Inventor	Richard W. Foote
Art Unit	2632
Examiner Name	Not Yet Assigned
Attorney Docket Number	P05792

Sheet 4

of

4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
SSF	DA	T. Yuzuriha et al., "Submicron Bipolar-CMOS Technology Using 16 Ghz ft Double Poly-Si Bipolar Devices", Tektronix, Inc. IEEE 1988, Pp. 748-751.	
SSF	DB	T. Yoshimura et al., "0.6 μ m High Speed BICMOS Technology with Emitter-Base Self-Aligned Structure", Fujitsu Limited, Bipolar IC Division, IEEE 1989, Pp. 241-244.	
SSF	DC	K. G. Moerschel et al., "Best: A BiCMOS-Compatible Super-Self-Aligned ECL Technology", AT&T Microelectronics, AT&T Bell Laboratories, IEEE 1990 Custom Integrated Circuits Conference, Pp. 18.3.1-18.3.4.	

Examiner
SignatureDate
Considered

8/21/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.